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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,800	01/04/2002	Lakshminarayan Viswanathan	125994	9182

7590 05/30/2003  
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EXAMINER

TRAN, MAI HUONG C

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 05/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/039,800

Applicant(s)

VISWANATHAN ET AL.

Examiner

Mai-Huong Tran

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 May 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) 23-28 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s): \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### **Election/Restriction**

Applicant's election with traverse of Group I (claims 1-22) in Paper No. 4 drawn to a semiconductor device is acknowledged. Accordingly, claims 23-28 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

The traversal is on the ground(s) that see the election paper. This is not found persuasive because the fields of search for method and device claims are NOT coextensive and the determinations of patentability of method and device claims are different, that is process limitations and device limitations are given weight differently in determining the patentability of the claimed inventions. Also, the strategies for doing text searching of the device claims and method claims are different. Thus, separate searches are required.

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

The requirement is still deemed proper and is therefore made **FINAL**.

**Claim Rejections - 35 U.S.C. § 102**

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 5-7 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 5,241,456 to Marcinkiewicz et al.

Regarding to claim 1, Marcinkiewicz et al. discloses a wire bond-less electronic component for use with a circuit external to the wire bond-less electronic component, the wire bond-less electronic component comprising a support substrate 12; an electronic device 26/36 over the support substrate 12; and a cover 64 located over the electronic device and the support substrate and comprising an interconnect structure 40/18 electrically coupled to the electronic device and adapted to electrically couple together the electronic device and the circuit for providing impedance transformation of an electrical signal between the electronic device and the circuit as set forth in col. 7, lines 45-68, col. 8, lines 1-19, col. 10, lines 12-23, figs 1, 6, and 7.

Regarding to claim 2, the wire bond-less electronic component wherein the interconnect structure is located within the cover (fig. 1).

Regarding to claim 3, the wire bond-less electronic component wherein the interconnect structure is located at a surface of the cover (fig. 1).

Regarding to claim 5, the wire bond-less electronic component wherein the wire bond-less electronic component is a surface mount device (fig. 1).

Regarding to claim 6, the wire bond-less electronic component wherein the cover is self-aligned to the support substrate (fig. 1).

Regarding to claim 7, the wire bond-less electronic component wherein the electronic device is located in a device substrate; and the cover is self-aligned to the device substrate (figs. 1 and 4).

### **Claim Rejections - 35 U.S.C. § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4 and 8-22 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 5,241,456 to Marcinkiewicz et al. in view of the remark.

Regarding to claim 4, Marcinkiewicz discloses the claimed invention except for the wire bond-less electronic component further comprising electrical leads located adjacent to the cover, wherein the interconnect structure electrically couples together the electronic device and the electrical leads; and the electrical leads electrically couple together the interconnect structure and the circuit. Marcinkiewicz discloses the external pins 68 instead of the electrical leads. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form electrical leads located adjacent to the cover, wherein the interconnect structure electrically couples together the electronic device and the electrical leads; and the electrical leads electrically couple together the interconnect structure and the circuit.

Regarding to claim 8, Marcinkiewicz et al. discloses the claimed invention except for the wire bond-less electronic component wherein the impedance transformation provided by the interconnect structure comprises a zero inductance ground potential for the electronic device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the wire bond-less electronic component wherein the impedance transformation provided by the interconnect structure comprises a zero inductance ground potential for the electronic device.

Claim 9 is rejected under the same rationale set forth above to claim 8.

Claim 10 is rejected under the same rationale set forth above to claim 1.

Claim 11 is rejected under the same rationale set forth above to claim 1.

Claim 12 is rejected under the same rationale set forth above to claim 1.

Claim 13 is rejected under the same rationale set forth above to claim 1.

Claim 14 is rejected under the same rationale set forth above to claim 1.

Regarding to claim 15, Marcinkiewicz et al. discloses a wire bond-less electronic component for use with a circuit external to the wire bond-less electronic component, the wire bond-less electronic component comprising a semiconductor substrate 12; a semiconductor device 26/36 supported by the semiconductor substrate 12; and a lid 66 located over the semiconductor device, the semiconductor substrate, the lid comprising a multi-functional interconnect system electrically coupled to the semiconductor device and electrically coupling together the semiconductor device and the circuit for providing a direct current to the semiconductor device and for providing impedance transformation of electrical signals from the semiconductor device to the circuit and from the circuit to the semiconductor device as set forth in cols. 7-8, 10 and figs 1 and 4.

Marcinkiewicz does not discloses a flange and a semiconductor substrate supported by the flange. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a flange and a semiconductor substrate supported by the flange.

Claim 16 is rejected under the same rationale set forth above to claim 15.

Claim 17 is rejected under the same rationale set forth above to claim 15.

Claim 18 is rejected under the same rationale set forth above to claim 15.

Claim 19 is rejected under the same rationale set forth above to claim 15.

Claim 20 is rejected under the same rationale set forth above to claim 15.


Claim 21 is rejected under the same rationale set forth above to claim 20.

Claim 22 is rejected under the same rationale set forth above to claim 20.

### Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (703) 305-1958. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (703) 308-4910.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

  
Mai-Huong Tran

  
HOAI HO  
PRIMARY EXAMINER